What is claimed is:

CLAIMS:

1. A WLAN (Wireless Local Area Network) receiver for receiving incoming radio signals, said WLAN receiver comprising a signal processing unit for processing received signals, said signal processing unit comprising:

   analog circuitry for performing analog signal processing; and

   digital circuitry for performing digital signal processing,

   wherein said signal processing unit further comprises:

   a header detection circuit for detecting a header in a received signal,

   wherein said analog circuitry comprises said header detection circuit.

2. The WLAN receiver of claim 1, wherein said analog circuitry is connected to said digital circuitry to provide a header detect signal to said digital circuitry in case a header is detected.

3. The WLAN receiver of claim 2, wherein said digital circuitry is arranged to operate, at least in part, in two operational modes, one of said at least two operational modes being less power consuming than the other one of said operational modes, said digital circuitry being capable of switching between said operational modes in response to said header detect signal.

4. The WLAN receiver of claim 3, wherein said digital circuitry is a arranged to enter said other one of said at least two operational modes in response to said header detect signal.

5. The WLAN receiver of claim 3, wherein said digital circuitry operable in two operational modes comprises at least one analog-to-digital converter for converting received analog radio signals to digital signals.

6. The WLAN receiver of claim 3, wherein said digital circuitry operable in two operational modes comprises a digital signal processor.

7. The WLAN receiver of claim 1 being IEEE 802.11g compliant.

8. The WLAN receiver of claim 1, wherein said header detection circuit is adapted to detect OFDM (Orthogonal Frequency Division Multiplexing) headers.

9. The WLAN receiver of claim 1, wherein said header detection circuit is adapted to detect CCK (Complementary Code Keying) headers.

10. The WLAN receiver of claim 1, wherein said signal processing unit is CMOS (Complementary Metal Oxide Semiconductor) implemented.

11. The WLAN receiver of claim 1, wherein said header detection circuit comprises a delay line for delaying the incoming radio signals.

12. The WLAN receiver of claim 11, wherein said header detection circuit further comprises a mixer unit for mixing the incoming radio signals with the delayed incoming radio signals to generate an autocorrelated mixer output signal.

13. The WLAN receiver of claim 12, wherein said mixer output signal is a complex mixer output signal.

14. The WLAN receiver of claim 12, wherein said header detection circuit further comprises a first integrator to integrate said mixer output signal.

15. The WLAN receiver of claim 14, wherein said first integrator is a passive second order low pass filter.

16. The WLAN receiver of claim 14, wherein said header detection circuit further comprises a rectifier unit for generating a signal representative of the absolute value of said integrated mixer output signal.

17. The WLAN receiver of claim 16, wherein said header detection circuit further comprises a reference path for generating a reference power signal based on the incoming radio signal.

18. The WLAN receiver of claim 17, wherein said reference path comprises a second integrator having integration characteristics corresponding to the integration characteristics of said first integrator.

19. The WLAN receiver of claim 17, wherein said header detection circuit further comprises a first comparator for comparing said signal representative of the absolute value of said integrated mixer output signal with a weighted reference power signal.

20. The WLAN receiver of claim 19, wherein the reference power signal is weighted by a scaling factor of approximately one-half.

21. The WLAN receiver of claim 19, wherein said first comparator is arranged for outputting a first control signal if said signal representative of the absolute value of said integrated mixer output signal is equal to or larger than said weighted reference power signal.

22. The WLAN receiver of claim 21, wherein said header detection circuit is arranged to provide a header detect signal to said digital circuitry based on said first control signal.

23. The WLAN receiver of claim 22, wherein said header detection circuit further comprises a third integrator for integrating said signal representative of the absolute value of said integrated mixer output signal.

24. The WLAN receiver of claim 23, wherein said third integrator has a longer integration time than said first integrator.

25. The WLAN receiver of claim 24, wherein said reference path comprises a fourth integrator having integration characteristics corresponding to the integration characteristics of said third integrator.

26. The WLAN receiver of claim 25, wherein said header detection circuit further comprises a second comparator (for comparing said signal representative of the absolute value of said integrated mixer output signal with an output of said fourth integrator.

27. The WLAN receiver of claim 26, wherein said header detection circuit is arranged for providing said header detect signal also based on an output of said second comparator.

28. The WLAN receiver of claim 25, wherein said header detection circuit further comprises a third comparator for comparing an output of said third integrator with a weighted output of said fourth integrator to provide a second header detect signal.

29. The WLAN receiver of claim 28, wherein the output of said fourth integrator is weighted by the same scaling factor as used for weighting said reference power signal.

30. The WLAN receiver of claim 28, wherein said digital circuitry comprises a signal latching unit for latching said header detect signal

and said second header detect signal, said signal latching unit having auto-reset capabilities.

31. The WLAN receiver of claim 30, wherein said header detection circuit is arranged to be reset in case of an AGC (Automatic Gain Control) reset.

32. The WLAN receiver of claim 30, wherein said header detection circuit is arranged to be reset when switching the WLAN receiver from a PLL (Phase Locked Loop) mode to a receiver mode.

33. The WLAN receiver of claim 1, wherein said header detection circuit is arranged to generate a header detect signal based on a first criterion and a second criterion, the first criterion defining that an autocorrelation value has to exceed a predefined fraction of the reception power, and the second criterion defining that the autocorrelation value has to exceed a predefined fraction of the integrated and delayed reception power.

34. The WLAN receiver of claim 1, wherein said incoming radio signal is a complex signal.

35. The WLAN receiver of claim 1, wherein said incoming radio signal is a bandpass signal.

36. The WLAN receiver of claim 35, wherein said header detection circuit comprises multiple autocorrelation stages each comprising a delay line and a mixer.

37. The WLAN receiver of claim 36, wherein said header detection circuit comprises a non-linear signal transformer between said autocorrelation stages.

38. An integrated circuit chip for processing signals received by a WLAN (Wireless Local Area Network) receiver, said integrated circuit chip comprising:

analog circuitry for performing analog signal processing; and

digital circuitry for performing digital signal processing,

wherein said integrated circuit chip further comprises:

a header detection circuit for detecting a header in a received signal,

wherein said analog circuitry comprises said header detection circuit.

39. A method of operating a WLAN (Wireless Local Area Network) receiver for processing incoming radio signals comprising:

performing analog signal processing; and

performing digital signal processing,

wherein said method further comprises:

detecting a header in a received signal,

wherein performing said analog signal processing comprises said header detection.